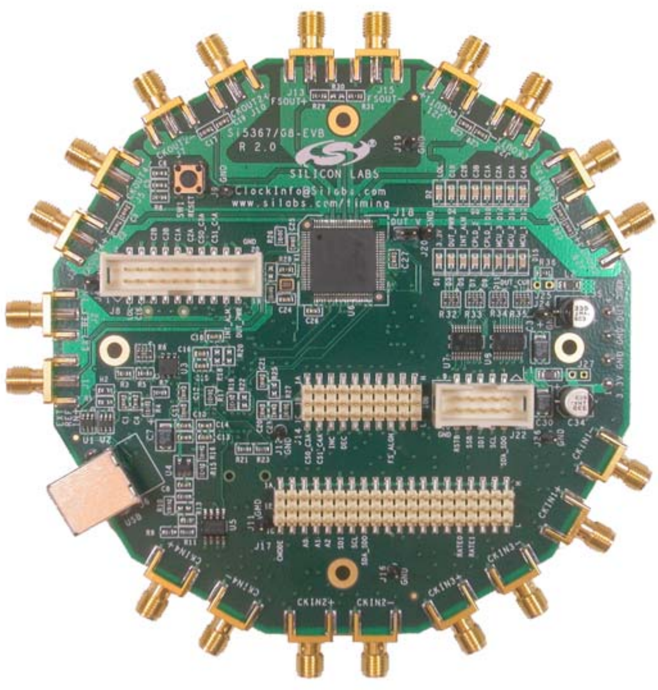
Si5365/66/67/68/69 Evaluation Board User's Guide

1. Introduction

The Si5365/66-EVB,Si5367/68-EVB, and Si5369-EVB provide platforms for evaluating Silicon Laboratories' Si5365/Si5366, Si5367/Si5368, and Si5369 Any-Frequency Precision Clocks. The Si5365 and Si5366 are controlled directly using configuration pins on the devices, while the Si5367, Si5368, and Si5369 are controlled by a microprocessor or MCU (microcontroller unit) via an I^{2}C or SPI interface. The Si5365 and Si5367 are low jitter clock multipliers with a loop bandwidth ranging from 30 kHz to 1.3 MHz. The Si5366 and Si5368 are jitter-attenuating clock multipliers, with a loop bandwidth ranging from 60 Hz to 8.4 kHz. The Si5369 is similar to the Si5368, with a much lower loop BW of from 4 to 525 Hz. The Si5366 device can optionally be configured to operate as a Si5365, so a single evaluation board is available to evaluate both devices. Likewise, the Si5368 can be configured to operate as a Si5367, so the two devices share a single evaluation board.

The Si5365/66/67/68/69 Any-Frequency Precision Clocks are based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The devices have excellent phase noise and jitter performance. The Si5366, Si5368, and Si5369 jitter attenuating clock multipliers support jitter generation of 0.3 ps RMS (typ) across the 12 kHz–20 MHz and 50 kHz–80 MHz jitter filter bandwidths. The Si5365 and SI5367 support jitter generation of 0.6 ps RMS (typ) across the 12 kHz–20 MHz and 50 kHz–80 MHz jitter filter bandwidths. For all devices, the DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. These devices are ideal for providing clock multiplication/clock division, jitter attenuation, and clock distribution in mid-range and high performance timing applications.


Top

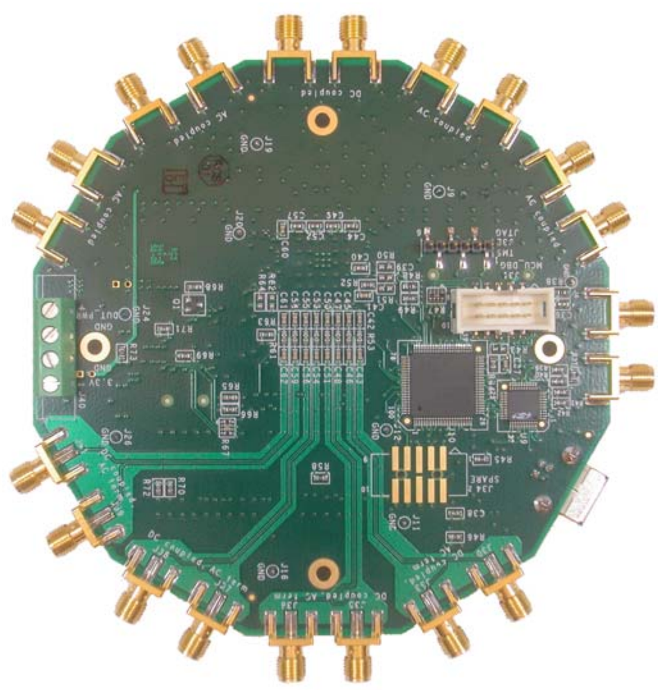

Bottom

Figure 1. Si536x TQFP EVB

Table 1. Features by Part Number

Device PN	# Clock Inputs	# Clock Outputs	Control	Input Freq (MHz)	Output Freq (MHz)	Jitter Generation (12 kHz–20 MHz)	Prog. Loop BW	Clock Mult.	Hitless Switching	Alarms	Package
Precision Clock Multipliers											
Si5365	4	5	Pin	15 to 707	19 to 1050	0.6 ps rms typ	30 kHz–1.3 MHz	Y	N	LOS, FOS	14 x 14 100-TQFP
Si5367	4	5	I^2C or SPI	10 to 710	10 to 1400	0.6 ps rms typ	30 kHz–1.3 MHz	Y	N	LOS, FOS	14 x 14 100-TQFP
Any-Frequency Precision Clock Multipliers with Jitter Attenuation											
Si5366	4	5	Pin	.008 to 707	.008 to 1050	0.3 ps rms typ	60 Hz–8.4 kHz	Y	Y	LOL, LOS, FOS	14 x 14 100-TQFP
Si5368	4	5	I^2C or SPI	.002 to 710	.002 to 1400	0.3 ps rms typ	60 Hz–8.4 kHz	Y	Y	LOL, LOS, FOS	14 x 14 100-TQFP
Si5369	4	5	I^2C or SPI	.002 to 710	.002 to 1400	0.3 ps rms typ	4 Hz–525 Hz	Y	Y	LOL, LOS, FOS	14 x 14 100-TQFP

2. Applications

The Si536x Any-Frequency Precision Clocks have a comprehensive feature set, including any-frequency synthesis, multiple clock inputs, multiple clock outputs, alarm and status outputs, hitless switching between input clocks, programmable output clock signal format (LVPECL, LVDS, CML, CMOS), output phase adjustment between output clocks, and output phase adjustment between all output clocks and the selected reference input clock (phase increment/decrement). For more details, consult the Silicon Laboratories timing products website at www.silabs.com/timing.

Both evaluation boards (EVBs) have a Silicon Laboratories MCU (C8051F340) that supports USB communications with a PC host. For the pin controlled parts (Si5365 and Si5366), the pin settings of the devices are determined by the MCU and the PC resident software that is provided with the EVB. For the MCU controlled parts (Si5367, Si5368, and Si5369), the devices are controlled and monitored through the serial port (either SPI or I^2C). A CPLD sits between the MCU and the Precision Clock device that performs voltage level translation and stores the pin configuration data for the pin controlled devices. Jumper plugs are provided so that the user can bypass the MCU/CPLD to manually control the pin controlled devices. Ribbon headers and SMA connectors are included so that external clock in, clock out and status pins can be easily accessed by the user. For the MCU controlled devices (Si5367, Si5368, and Si5369)), the user also has the option of bypassing the MCU and controlling the parts from an external serial device. On-board termination is included so that the user can evaluate either single-ended or differential as well as ac or dc coupled clock inputs and outputs. A separate DUT (device under test) power supply connector is included so that the Precision Clocks can be run at either 1.8, 2.5, or 3.3 V, while the USB MCU remains at 3.3 V. LEDs are provided for convenient monitoring of key status signals.

For more detailed information about these devices, refer to the Any-Frequency Precision Clock Family Reference Manual.

3. Features

The Si5365/66-EVB, Si5367/68-EVB, and Si5369-EVBs each include the following:

- CD with documentation and EVB software including the DSPLL*sim* configuration software utility
- USB cable
- EVB circuit board including a Si5366 (Si5365/66-EVB), a Si5368 (Si5367/68-EVB), or a Si5369 (Si5369-EVB)
- User's Guide (this document)

4. Si5365/66-EVB, Si5367/68-EVB, and Si5369-EVB Quick Start

1. Install the Precision Clock EVB Driver. (This must be installed before the EVB is connected to the PC via the USB cable.) For details, see Section "7.EVB Software Installation" on page 12.
2. Install the Precision Clock EVB Software. (Assumes that Microsoft .NET Framework 3.1 is already installed.)
3. Connect the two power supplies to the EVB. One is 3.3 V and the other is either 1.8, 2.5, or 3.3 V. The DUT is powered by the 1.8/2.5/3.3 V supply.
4. Turn on the power supplies.
5. Connect a USB cable from the EVB to the PC where the software was installed.
6. Install USB driver.
7. Launch software by clicking on **Start→Programs→Silicon Laboratories→Precision Clock EVB Software** and selecting one of the programs.

5. Functional Description

The Si5365/66-EVB, Si5367/68-EVB, Si5369-EVB, and DSPLL*sim* software allow for a complete and simple evaluation of the functions, features, and performance of the Si536x Any-Frequency Precision Clocks.

5.1. Narrowband versus Wideband Operation

This document describes three evaluation boards: one for the Si5365 and Si5366, another for the Si5367 and Si5368, and a third for the Si5369. The first evaluation board is for pin controlled clock parts, the second is for clock parts that are to be controlled by an MCU over a serial port, and the third is for a very low loop bandwidth device that is also controlled by an MCU. Two of the boards supports two parts: one that is wideband (the Si5365 and the Si5367) and the one that is narrowband (the Si5366 and the Si5368). The third board only supports the low loop bandwidth narrowband Si5369. The narrowband parts other than the Si5369 are both capable of operating in the wideband mode, so evaluation of the wideband parts can be done by using a narrowband part in wideband mode. As such, these evaluation boards are only populated with narrowband parts.

To evaluate Si5365 device operation using the Si5365/66-EVB, the RATE[1:0] pins must be set to HH using the jumper provided. To evaluate Si5367 device operation using the Si5367/68-EVB, the Precision Clock EVB Software should be configured for wideband mode. For details, see the Precision Clock EVB Software documentation that can be found on the enclosed distribution CD.

5.2. Block Diagram

Figure 2 is a block diagram of the evaluation board. The MCU communicates to the host PC over a USB connection. The MCU controls and monitors the Si536x through the CPLD. The CPLD, among other tasks, translates the signals at the MCU voltage level of 3.3 V to the Si536x's voltage level, which is nominally 3.3, 2.5, or 1.8 V. The user has access to all of the Si536x's pins using the various jumper settings as well as through the host PC via the MCU and CPLD.

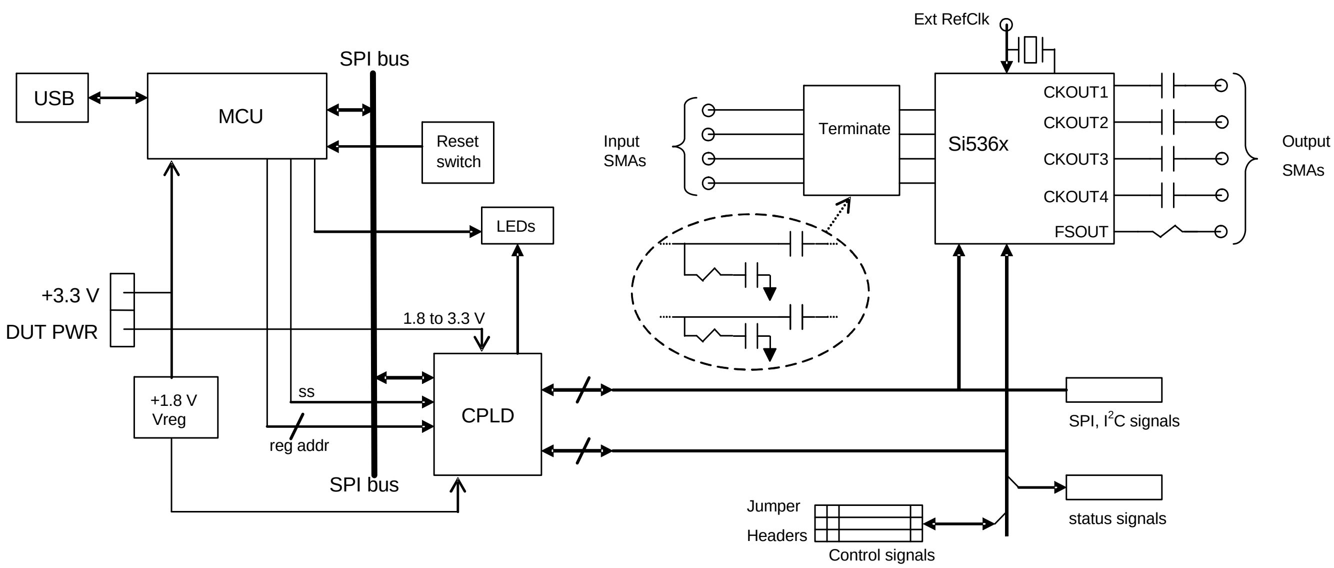


Figure 2. Si536x TQFP Block Diagram

5.3. Si536x Input and Output Clocks

The Si536x has four differential inputs that are ac terminated to 50 Ω and then ac coupled to the part. Single ended operation can be implemented by simply not connecting to one of the two of the differential pairs. When operating with clock inputs of 1 MHz or less in frequency, the appropriate dc blocking capacitors (C58, C61, C47, C50, C53, C55, C42 and C45) located on the bottom of the board should be replaced with zero ohm resistors. The reason for this is that the capacitive reactance of the ac coupling capacitors becomes significant at low frequencies. It is also important that the CKIN signal meet the minumum rise time of 11 ns (CKNtrf) even though the input frequency is low.

The four clock outputs are all differential, ac coupled and configured for driving 50 Ω transmission lines. **When using single ended outputs, it is important that the unused half of the output be terminated**. Given that the Frame Sync signal can have a duty cycle that is far from 50%, the Frame Sync outputs are dc coupled. If the Frame Sync or other clock ouputs signals are configured for CMOS, then the two outputs are not complements of one another and should be wired in parallel so that the output drive current is doubled. To evaluate CMOS level Frame Sync outputs, a 0 Ω resistor should be installed at R19. Note that for the MCU controlled parts that support Frame Sync mode (Si5367 and Si5368), the Frame Sync output signal format can be configured independently of the other four outputs.

Two jumpers are provided to assist in monitoring the Si536x power. When R36 is removed, J25 can be used to measure the device current. J18 can be used at any time to monitor the supply voltage at the device.

The Si5366, Si5368, and Si5369 require that an external reference clock be provided to enable the devices to operate as narrowband jitter attenuators with loop bandwidths as low as 60 Hz (as low as 4 Hz for the Si5369). The external reference clock can be either a crystal, a stand-alone oscillator or some other clock source. The range of acceptable reference frequencies is described in the Any-Frequency Precision Clocks Family Reference Manual (Si53xx-RM). The EVB's are shipped with a 3rd overtone 114.285 MHz crystal that is used in the majority of applications. J1 and J2 are used when the Si536x is to be configured in narrowband mode with an external reference oscillator (i.e., without using the 114.285 MHz crystal).

The RATE pins should also be configured for the desired mode, either through DSPLL*sim* or using the jumper plugs at J17 (see Table 7 on page 11).

Table 2 shows how the various components should be configured for the three modes of operation:

Table 2. Reference Input Mode

	Mode		
	Xtal[1]	**38.88 MHz Ext Ref**[2]	**Wideband**
Input 1	NC[3]	J1	NC
Input 2	NC	J2	NC
C39	NOPOP[4]	install	install
C22	NOPOP	install	NOPOP
R50	NOPOP	NOPOP	install
R28	install	NOPOP	NOPOP
RATE0	M	—	H
RATE1	M	—	H

Notes:
1. Xtal is 114.285 MHz 3rd overtone.
2. For external reference frequencies and RATE pin settings, see the Any-Frequency Precision Clock Family Reference Manual.
3. NC—no connect.
4. NOPOP—do not install this component.

For a differential external reference, connect the balanced input signals to J1 and J2. For single-ended operation, connect the input signal to J1 and disconnect J2.

R51 is provided so that a different termination scheme can be used. If R51 is populated, then remove R52 and R24.

5.4. CPLD

This CPLD is required for the MCU to control an Si536x operating at either 1.8, 2.5, or 3.3 V. The CPLD provides two main functions: it translates the voltage level from 3.3 V (the MCU voltage) to the Si536x voltage (either 1.8, 2.5, or 3.3 V). The MCU communicates to the CPLD with the SPI signals SS_CPLD_B (slave select), MISO (master in, slave out), MOSI (master out, slave in) and SCLK. The MCU can talk to CPLD-resident registers that are connected to pins that control the Si536x's pins, mainly for pin control mode. When the MCU wishes to access a Si536x register, the SPI signals are passed through the CPLD, while being level translated, to the Si536x. The CPLD is an EE device that is retains its code that is loaded through the JTAG port (J32). The core of the CPLD runs at 1.8 V, which is provided by voltage regulator U4. The CPLD also logically connects many of the LEDs to the appropriate Si536x pins.

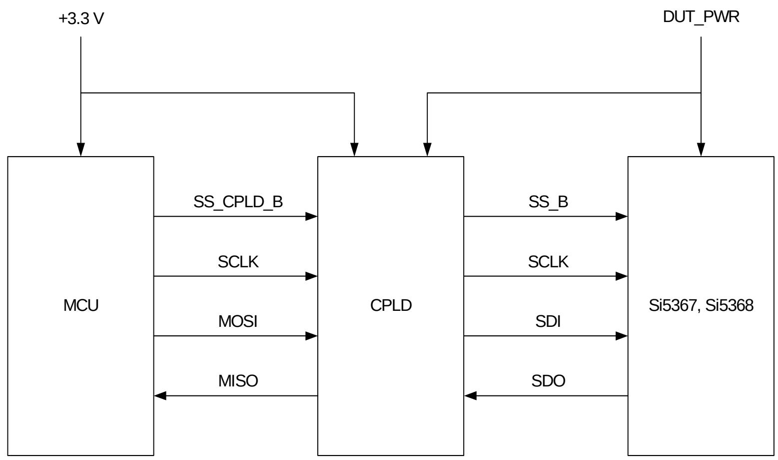


Figure 3. SPI Mode Serial Data Flow

5.5. MCU

The MCU communicates with the PC over USB so that PC resident software can be used to control and monitor the Si536x. The USB connector is J6 and the debug port, by which the MCU is flashed, is J31. The reset switch, SW1, resets the MCU, but not the CPLD. The MCU is a self-contained USB master and runs all of the code required to control and monitor the Si536x, both in the MCU mode and in the pin-controlled modes.

U3 contains a unique serial number for each board and U5 is an EEPROM that is used to store configuration information for the board. The board powers up in free run mode with a configuration that is outlined in "Appendix—Powerup and Factory Default Settings" on page 26. For the pin controlled parts (Si5365/66-EVB), the contents of U5 configure the board on power up so that jumper plugs may be used. If DSPLLsim is subsequently run, the jumper plugs should be removed before DSPLLsim downloads the configuration to the EVB so that the jumpers do not conflict with the CPLD outputs. For microprocessor parts, U5 configures the EVB for a specific frequency plan as described in "Appendix—Powerup and Factory Default Settings" on page 26.

The Evaluation board has a serial port connector (J22) that supports the following:

- Control by the MCU/CPLD of an Any-Frequency part on an external target board.
- Control of the Any-Frequency part that is on the Evaluation board through an external SPI or I^2C port.

For details, see J22 (Table 6).

Though they are not needed on this Evaluation Board because the CPLD has low output leakage current, some applications will require the use of external pullup and pulldown resistors when three level pins are being driven by external logic drivers. This is particularly true for the pin-controlled parts: the Si5365 and Si5367. Consult the Si53xx-RM Any-Frequency Precision Clock Family Reference Manual for details.

LVPECL outputs will not function at 1.8 V. If the Si536x part is to be operated at 1.8 V, the output format needs to be changed by altering either the SFOUT pins (Si5365/66) or the SFOUT register bits (Si5367/68/69).

5.6. Power and 2L Signals

This evaluation board requires two power inputs +3.3 V for the MCU and either 1.8, 2.5, or 3.3 V for the Any-Frequency Precision Clock part. The power connector is J40. The grounds for the two supplies are tied together on the EVB. There are sixteen LEDs, as described in Table 3. J14 is a three by 10 pin male header by which the user can manually set the values of the two-level inputs using jumper plugs connected to either ground (silkscreen labeled L) or the power supply (labeled H). J8 is a twenty pin ribbon header that brings out all of the status outputs from the Si536x. Note that some pins are shared and serve as both inputs and outputs, depending on how the device is configured. For users that wish to remotely access the input and output pins settings with external hardware, J14 and J8 can be connected to ribbon cables.

5.7. 3L Pins

The three-level inputs can all be manually configured by installing jumper plugs at J17, either H or L. The M level is achieved by not installing a jumper plug at a given location. J17 can also be used as a connection to an external circuit that controls these pins. J22 is a ten pin ribbon header that is provided so that an external processor can control the Si536x over either the SPI or I^2C bus.

6. Connectors and LEDs

6.1. LEDs

There are sixteen LEDs on the board which provide a quick and convenient means of determining board status.

Table 3. LED Status and Description

LED	Color	Label	LED	Color	Label
D1	green	3.3 V	D2	red	LOL
D3	green	DUT_PWR	D4	red	C1B
D5	red	ALRMOUT	D6	red	C2B
D7	yellow	CPLD_2	D8	red	C3B
D9	yellow	CPLD_1	D10	green	C1A
D11	red	MCU_3	D12	green	C2A
D13	red	MCU_2	D14	green	C3A
D15	red	MCU_1	D16	green	C4A

6.2. User Jumpers and Headers.

Use Figure 4 to locate the jumpers described in Tables 4, 5, 6, and 7:

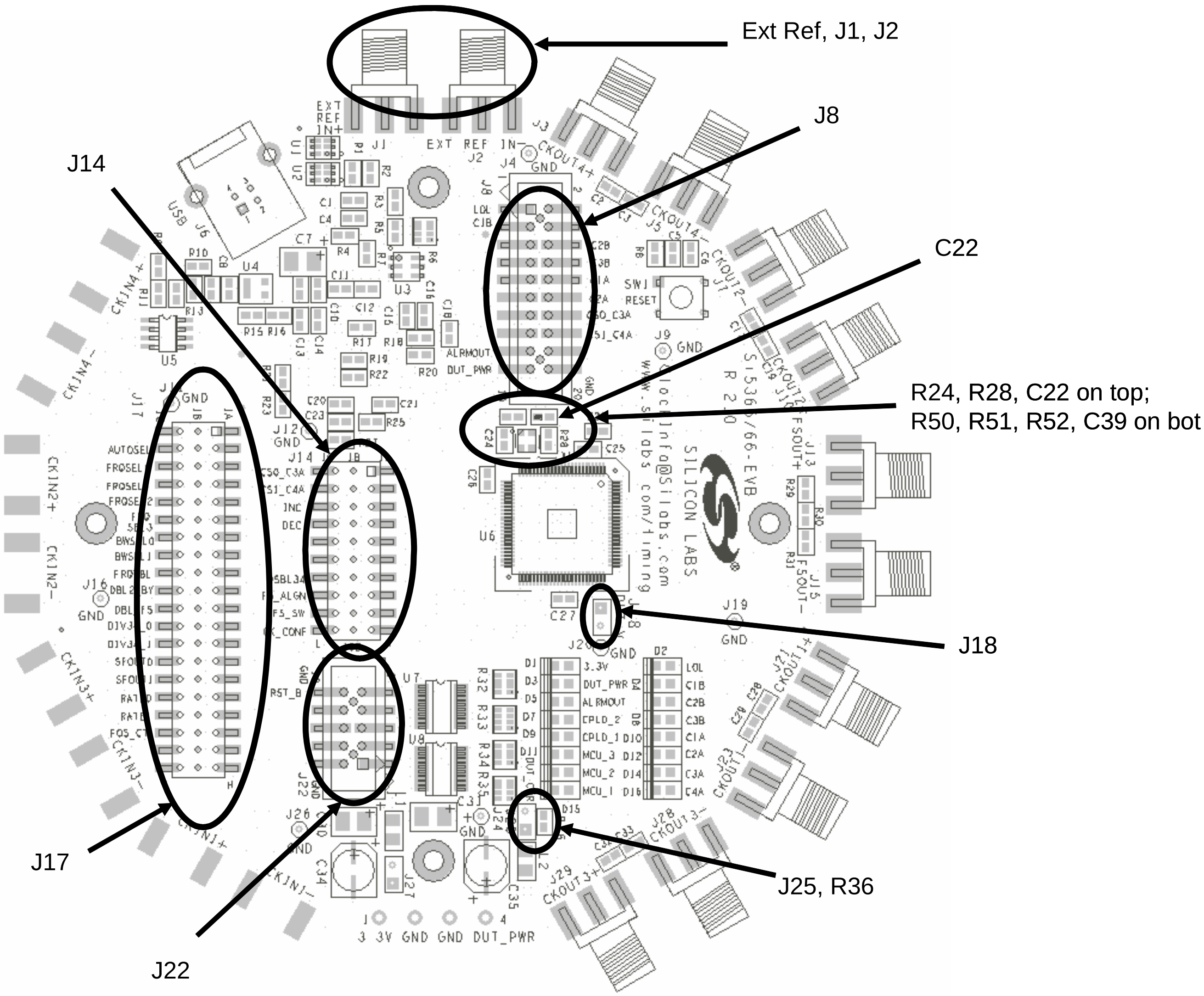


Figure 4. Connectors, Jumper Header Locations

J25 assists in measuring the Any-Frequency Precision Clock current draw. If J25 is to be used, R36 should be removed.

J14 is a three-pin by ten header that is used to establish input levels for the pin controlled two-level inputs using jumper plugs. It also provides a means of externally driving the two-level input signals:

Table 4. Two-Level Input Jumper Header, J14

J36	Pin	Comment
J14.1B	CS0_C3A	CS0
J14.2B	CS1_C4A	CS1
J14.3B	INC	
J14.4B	DEC	
J14.5B	—	not used
J14.6B	—	not used
J14.7B	DSBL34	
J14.8B	FS_ALIGN	
J14.9B	FS_SW	
J14.10B	CK_CONF	

J8 is a 20 pin ribbon header that provides an external path to monitor the status pins.

Table 5. External Status Connector, J8

J37	Pin	Comment
J8.1	LOL	
J8.3	C1B	
J8.5	C2B	
J8.7	C3B	
J8.9	C1A	
J8.11	C2A	
J8.13	CS0_C3A	C3A
J8.15	CS1_C4A	C4A
J8.17	INT_ALRM	
J8.19	DUT_PWR	

J22 is a 10 pin ribbon header that provides an external path to serially communicate with the Any-Frequency Precision Clock.

To control the Any-Frequency part that is on the Evaluation Board from an external serial port, open the Register Programmer, connect to the Evaluation Board, go to Options in the top toolbar and select "Switch To External Control Mode".

To control an Any-Frequency part that is on an external target board from the Evaluation Board using its serial port, tie pin 9 of J22 low so that the on-board Any-Frequency part is constantly being held in reset. This will force it to disable its SDA_SDO output buffer.

Table 6. External Serial Port Connector, J22

J38	Pin	Comment
J22.1	SDA_SDO	
J22.3	SCL_SCLK	
J22.5	SDI	
J22.7	A2_SS	
J22.9	DUT_RST_B	reset

J17 is a three-pin by twenty header that is used to establish input levels for the pin controlled three-level inputs using jumper plugs. It also provides a means of externally driving the three-level input signals.

Table 7. Three-Level Input Jumper Headers, J17

J39	Pin	Comment
J17.1B	CMODE	
J17.2B	AUTOSEL	
J17.3B	A0_FRQSEL0	
J17.4B	A1_FRQSEL1	
J17.5B	A2_SS_FRQSEL2	
J17.6B	SDI_FRQSEL3	
J17.7B	SCL_SCLK_BWSEL0	
J17.8B	SDA_SDO_BWSEL1	
J17.9B	FRQTBL	
J17.10B	DBL2_BY	
J17.11B	BDBL_FS	
J17.12B	DIV34_0	
J17.13B	DIV34_1	
J17.14B	SFOUT0	
J17.15B	SFOUT1	
J17.16B	RATE0	
J17.17B	RATE1	
J17.18B	FOS_CTL	
J17.19B	—	not used
J17.20B	—	not used

J18 is used to monitor the Any-Frequency Precision Clock voltage.

J1 and J2 are edge mount SMA connectors that are used, if so configured, to supply an external single-ended or differential reference oscillator.

7. EVB Software Installation

The release notes and the procedure for installing the EVB software can be found on the release CD included with the EVB. These items can also be downloaded from the Silabs web site: www.silabs.com/timing. Follow the links for 1-PLL Jitter attenuators, and look under the Tools tab.

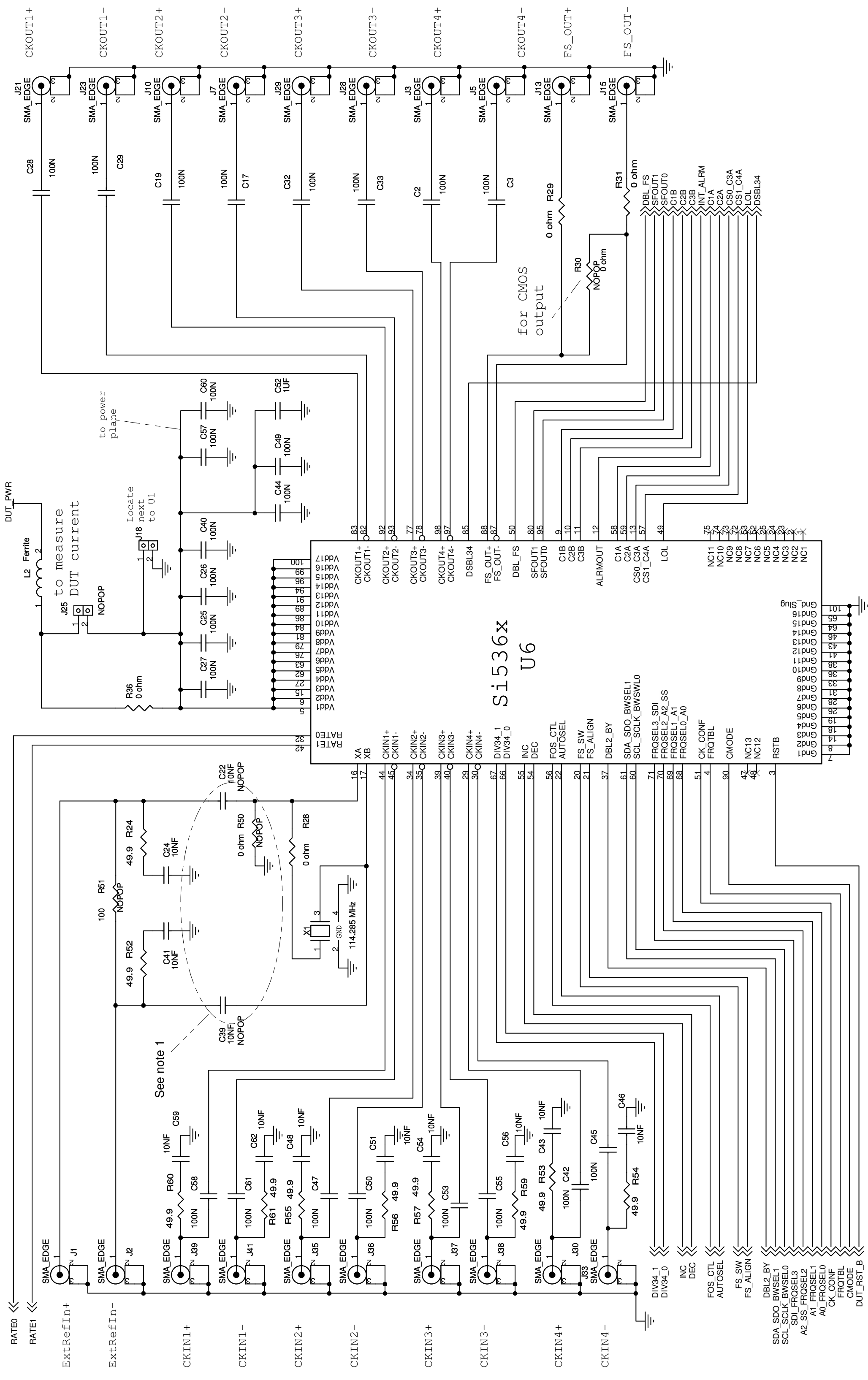
7.1. Precision Clock EVB Software Description

There are several programs to control the Precision Clock device. Each provides a different kind of access to the device. Refer to the online help in each program by clicking **Help→Help** in the menu for more information on how to use the software. Note: Some of the Precision Clock devices do not have a register map, so some programs may not be applicable to them.

Table 8. User Applications

Program	Description
Register Viewer	The Register Viewer displays the current register map data in a table format sorted by register address to provide an overview of the device's state. This program can save and print the register map.
Register Programmer	The Register Programmer provides low-level register control of the device. Single and batch operations are provided to read from and write to the device. Register map files can be saved and opened in the batch mode.
Setting Utility	This application allows for quick access to each control on the Precision Clock device (either pin- or register-based). It can save and open text files as well.
DSPLL*sim*	The DSPLL*sim* provides high-level control of the Precision Clock device. It has the frequency planning wizard as well as control of the pins and registers in a organized, intuitive manner.

8. Schematics



Notes:

1. Change for Si5365, Si5367, and External Reference.

Figure 5. Si536x

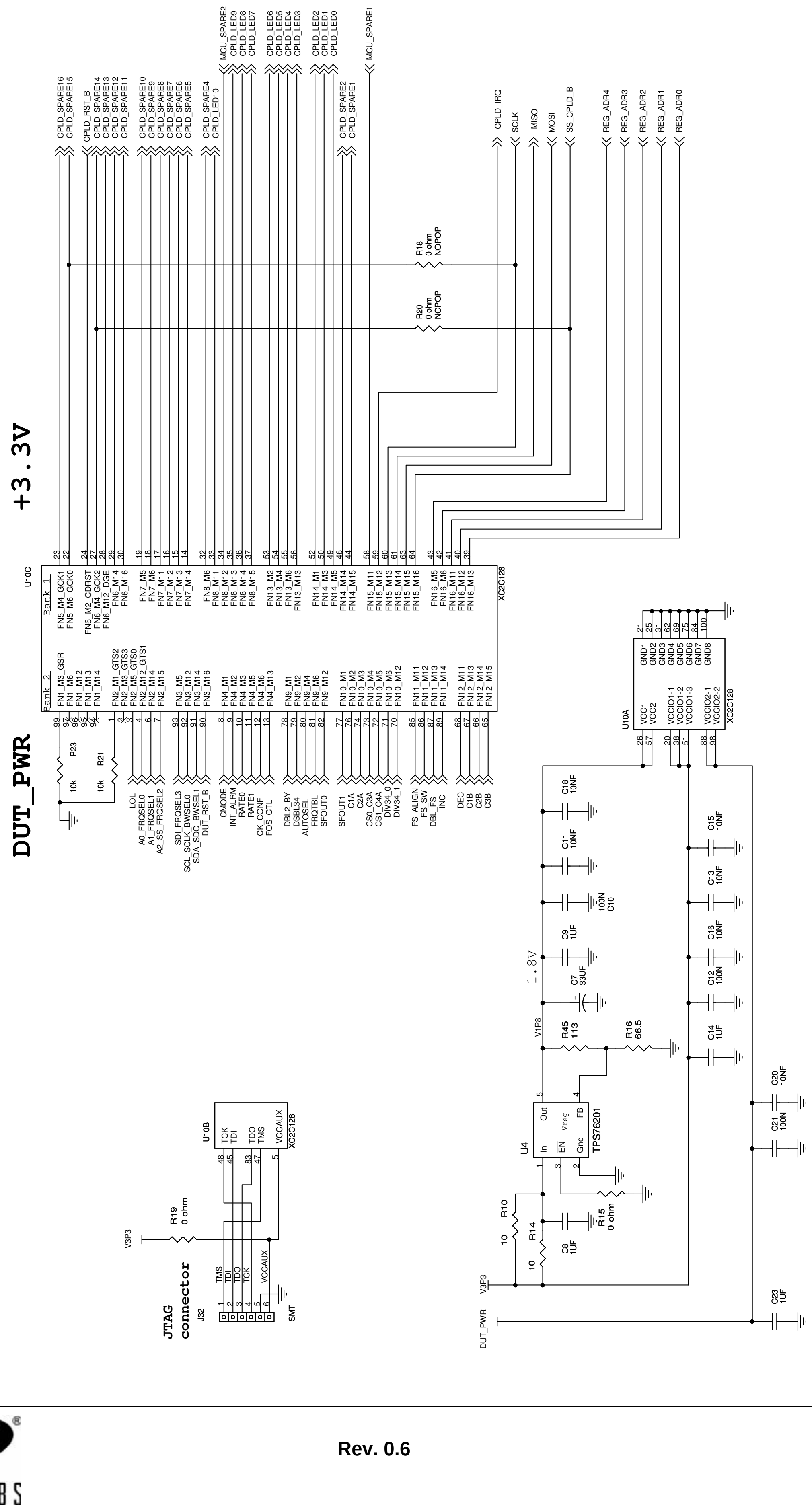


Figure 6. CPLD

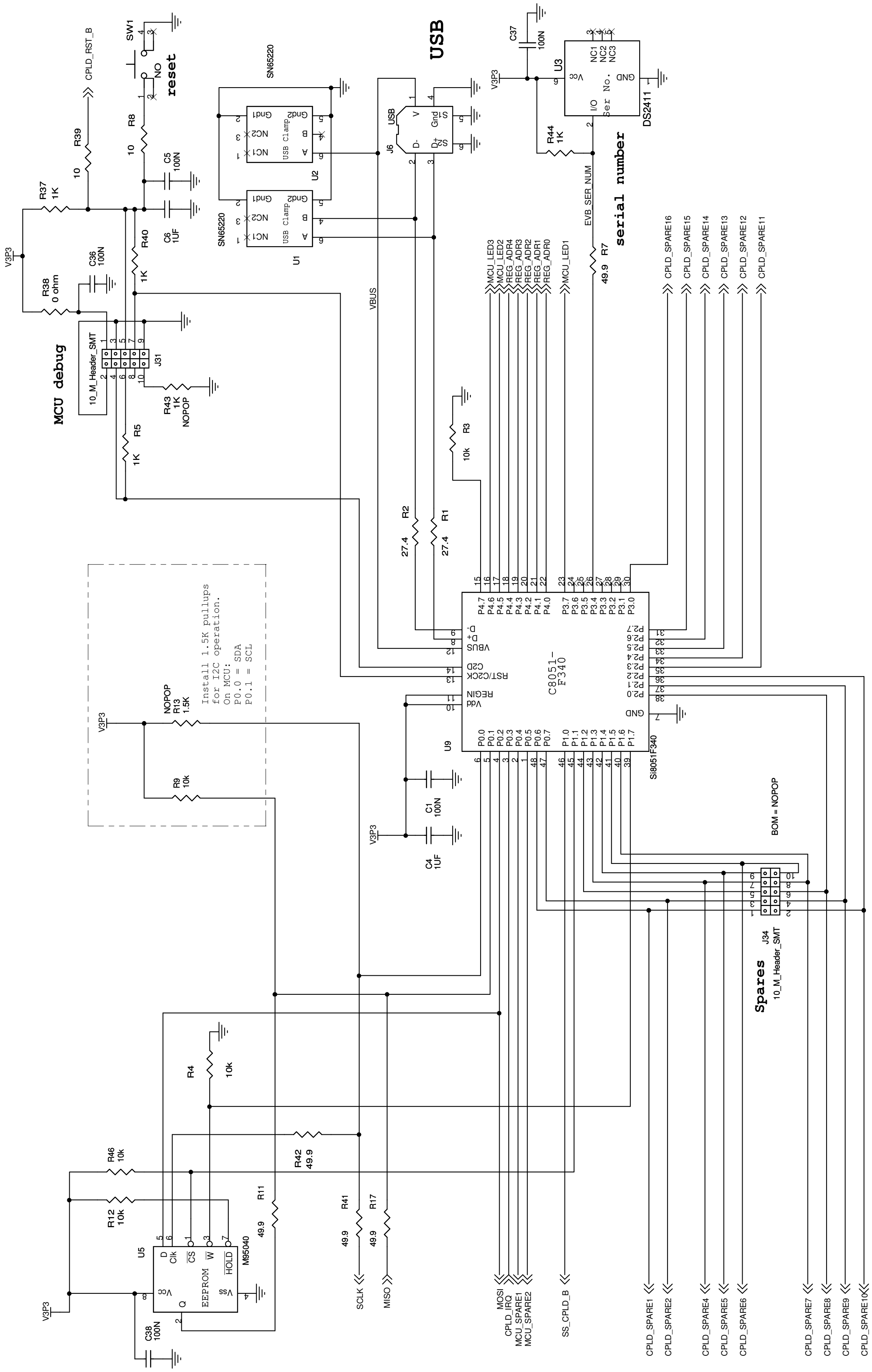

USB
reset
serial number
MCU debug
Spares
SW1
CPLD_RST_B
R39
R37
1K
R38
0 ohm
C36
100N
R8
C5
100N
C6
1UF
R40
1K
J31
10_M_Header_SMT
R43
1K
NOPOP
R5
1K
U1
U2
SN65220
USB Clamp
J6
VBUS
R2
27.4
R1
27.4
R3
10k
C37
100N
U3
DS2411
Ser No.
R44
1K
EVB_SER_NUM
R7
49.9
MCU_LED3
MCU_LED2
REG_ADR4
REG_ADR3
REG_ADR2
REG_ADR1
REG_ADR0
MCU_LED1
CPLD_SPARE16
CPLD_SPARE15
CPLD_SPARE14
CPLD_SPARE13
CPLD_SPARE12
CPLD_SPARE11
C8051-F340
U9
Si8051F340
Install 1.5K pullups
for I2C operation.
On MCU:
P0.0 = SDA
P0.1 = SCL
NOPOP
R13
1.5K
R9
10k
V3P3
C1
100N
C4
1UF
BOM = NOPOP
J34
10_M_Header_SMT
R4
10k
R46
10k
R12
10K
R42
49.9
R11
49.9
U5
M95040
EEPROM
C38
100N
R41
49.9
R17
49.9
SCLK
MISO
MOSI
CPLD_IRQ
MCU_SPARE1
MCU_SPARE2
SS_CPLD_B
CPLD_SPARE1
CPLD_SPARE2
CPLD_SPARE4
CPLD_SPARE5
CPLD_SPARE6
CPLD_SPARE7
CPLD_SPARE8
CPLD_SPARE9
CPLD_SPARE10

Figure 7. MCU

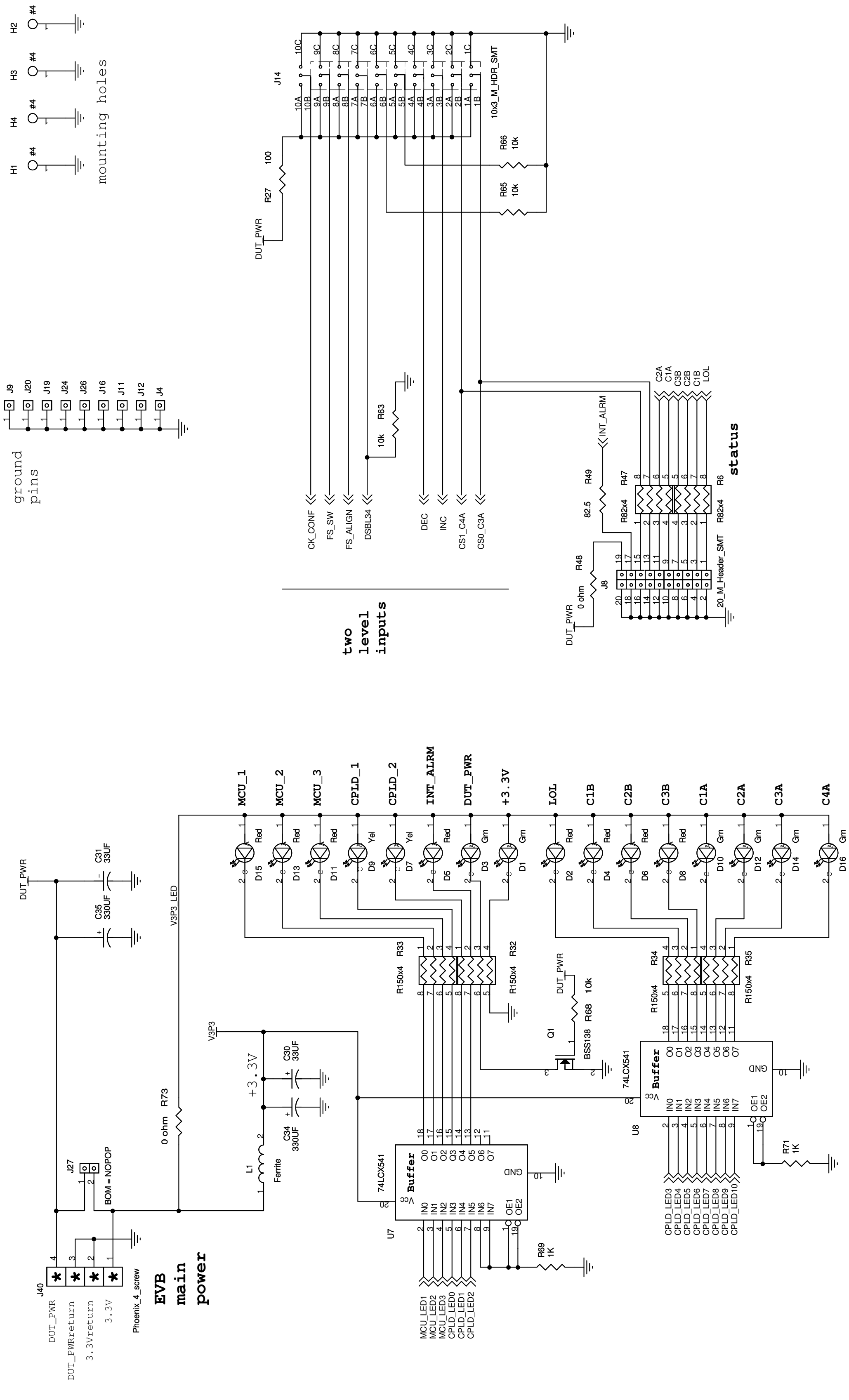
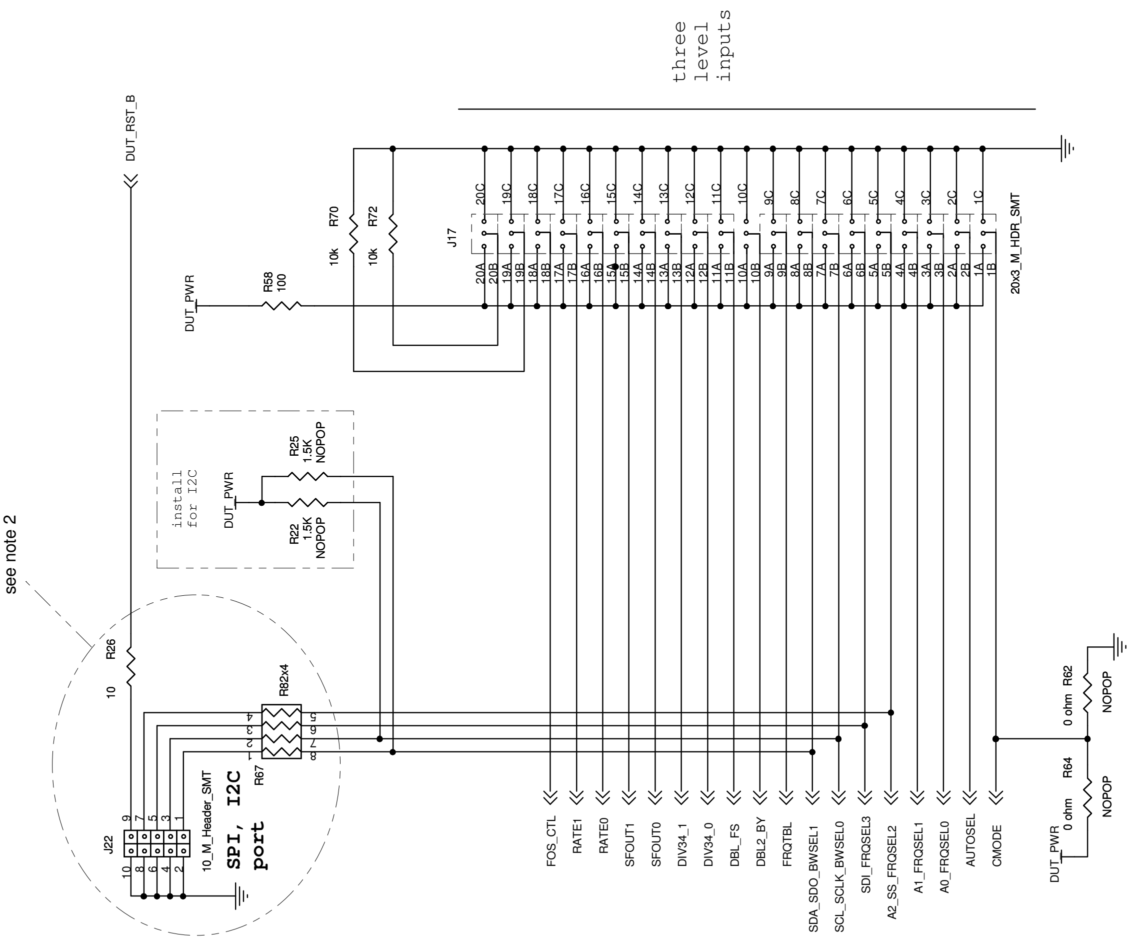


Figure 8. Power, LEDs and 2L Inputs



Notes:

2. NOPOP for Si5365 and Si55366.

Figure 9. Serial Port, 3L Inputs

9. Bill of Materials

Table 9. Si536x Bill of Materials

Item	Qty	Reference	Part	Mfgr	MfgrPartNum
1	32	C1,C2,C3,C5,C10,C12,C17,C19,C21,C25,C26,C27,C28,C29,C32,C33,C36,C37,C38,C40,C42,C44,C45,C47,C49,C50,C53,C55,C57,C58,C60,C61	100 N	Venkel	C0603X7R160-104KNE
2	7	C4,C6,C8,C9,C14,C23,C52	1 UF	Venkel	C0603X7R6R3-105KNE
3	3	C7,C30,C31	33 UF	Venkel	TA0006TCM336MBR
4	16	C11,C13,C15,C16,C18,C20,C24,C41,C43,C46,C48,C51,C54,C56,C59,C62	10 NF	Venkel	C0603X7R160-103KNE
6	2	C34,C35	330 UF	Panasonic	EEE-HA0J331XP
7	6	D1,D3,D10,D12,D14,D16	Grn	Lumex	SML-LXT0805GW-TR
8	8	D2,D4,D5,D6,D8,D11,D13,D15	Red	Lumex	SML-LXT0805SRW-TR
9	2	D7,D9	Yel	Lumex	SML-LXT0805YW-TR
10	4	H1,H2,H3,H4	#4 mounting hole		
11	20	J1,J2,J3,J5,J7,J10,J13,J15,J21,J23,J28,J29,J30,J33,J35,J36,J37,J38,J39,J41	SMA_EDGE	Johnson	142-0701-801
12	9	J4,J9,J11,J12,J16,J19,J20,J24,J26	Jmpr_1pin		
13	1	J6	USB	FCI	61729-0010BLF
14	1	J8	20_M_Header_SMT	Samtec	HTST-110-01-lm-dv-a
15	1	J14	10x3_M_HDR_SMT	Samtec	TSM-110-01-L-TV
16	1	J17	20x3_M_HDR_SMT	Samtec	TSM-120-01-L-TV
17	1	J18	Jmpr_2pin		
18	1	J22	10_M_Header_SMT	Samtec	HTST-105-01-lm-dv-a
20	1	J31	10_M_Header_SMT	Samtec	HTST-105-01-lm-dv-a
21	1	J32	SMT	Sullins	GZC36SABN-M30
23	1	J40	Phoenix_4_screw	Phoenix	MKDSN 1.5/4-5.08
24	2	L1,L2	Ferrite	Venkel	FBC1206-471H
25	1	Q1	BSS138	On Semi	BSS138LT1G
26	2	R1,R2	27.4	Venkel	CR0603-16W-27R4FT
27	13	R3,R4,R9,R12,R21,R23,R46,R63,R65,R66,R68,R70,R72	10 k	Venkel	CR603-16W-1002FT
28	6	R5,R37,R40,R44,R69,R71	1 K	Venkel	CR0603-16W-1001FT
29	3	R6,R47,R67	R82x4	Panasonic	EXB-38V820JV
30	15	R7,R11,R17,R24,R41,R42,R52,R53,R54,R55,R56,R57,R59,R60,R61	49.9	Venkel	CR0603-16W-49R9FT

Table 9. Si536x Bill of Materials (Continued)

Item	Qty	Reference	Part	Mfgr	MfgrPartNum
31	5	R8,R10,R14,R26,R39	10	Venkel	CR0603-16W-10R0FT
33	9	R15,R19,R28,R29,R31,R36,R38, R48,R73	0 ohm	Venkel	CR0603-16W-000T
34	1	R16	66.5	Venkel	CR0603-16W-66R5FT
36	2	R27,R58	100	Venkel	CR0603-16W-1000FT
37	4	R32,R33,R34,R35	R150x4	Panasonic	EXB-38V151JV
39	1	R45	113	Venkel	CR0603-16W-1130FT
40	1	R49	82.5	Venkel	CR0603-16W-82R5FT
42	1	SW1	NO	Mountain Switch	101-0161-EV
43	2	U1,U2	SN65220	TI	SN65220DBVT
44	1	U3	DS2411	Maxim/Dallas	DS2411P
45	1	U4	TPS76201	TI	TPS76201DBVT
46	1	U5	M95040	ST Micro	M95040-WMN6P
47	1	U6	Si5368A-X-GQ*	Silicon Labs	Si5368A-X-GQ
48	2	U7,U8	74LCX541	Fairchild	74LCX541MTC_NL
49	1	U9	Si8051F340	Silicon Labs	C8051F340-GQ
50	1	U10	XC2C128	Xilinx	XC2C128-7VQG100I
51	1	X1 for Si5365/66-EVB and Si5367/68-EVB	114.285 MHz	TXC	7MA1400014
51	1	X1 for the Si5369-EVB	114.285 MHz, 20 ppm	NDK	EX500A-C500997
Not Populated					
5	2	C22,C39	10 NF	Venkel	C0603X7R160-103KNE
19	2	J25,J27	Jmpr_2pin		
22	1	J34	10_M_Header_SMT	Samtec	HTST-105-01-lm-dv-a
32	3	R13,R22,R25	1.5 K	Venkel	CR0603-16W-1501FT
35	6	R18,R20,R30,R50,R62,R64	0 ohm	Venkel	CR0603-16W-000T
38	1	R43	1 K	Venkel	CR0603-16W-1001FT
41	1	R51	100	Venkel	CR0603-16W-1000FT

***Note:** X denotes the product revision. Consult the ordering guide in the Si5368 Data Sheet for the latest product revision. For the Si5365/66-EVB, substitute Si5366-C-GQ. For the Si5369-EVB, substitute Si5369A-C-GQ.

10. Layout

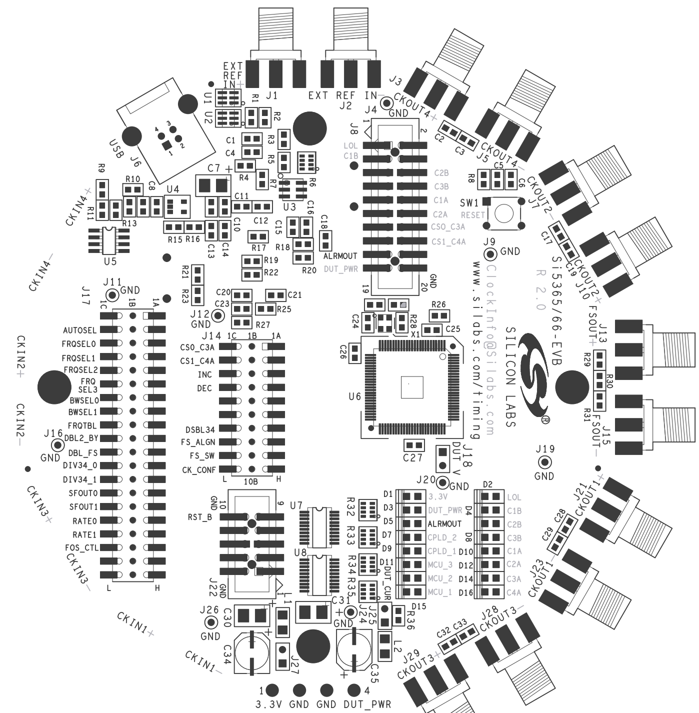


Figure 10. Silkscreen Top

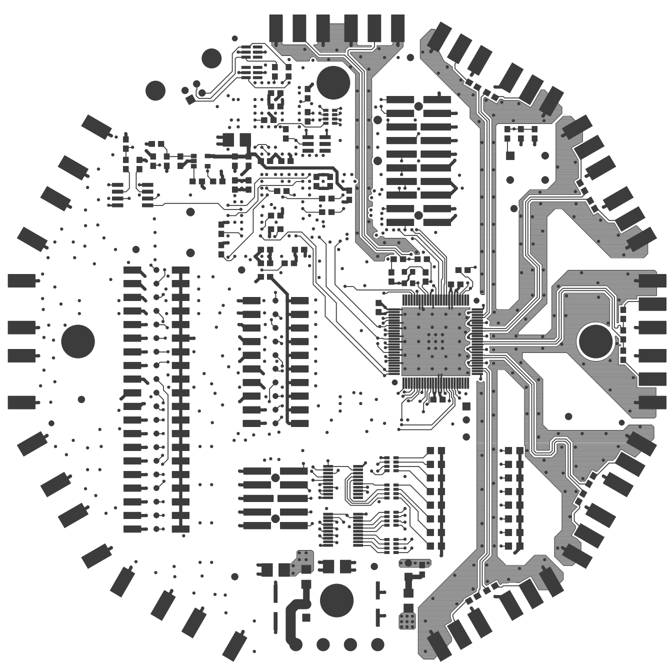


Figure 11. Layer 1

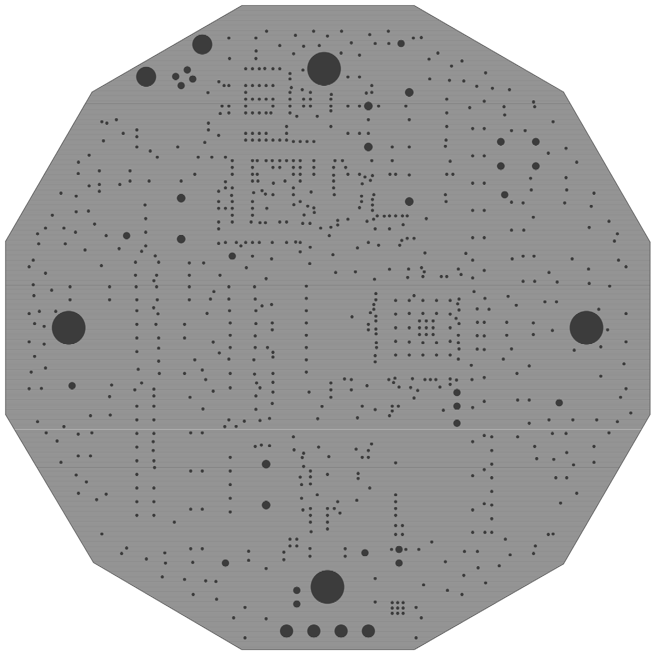


Figure 12. Layer 2, Ground Plane

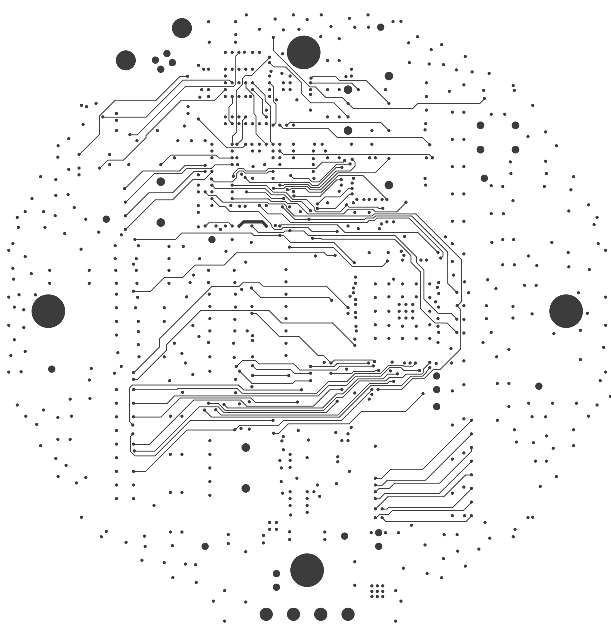


Figure 13. Layer 3

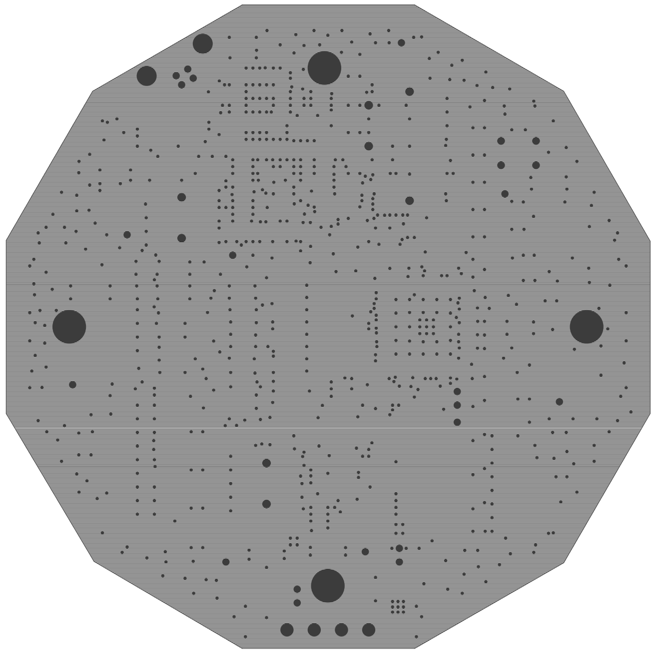


Figure 14. Layer 4, 3.3 V Power

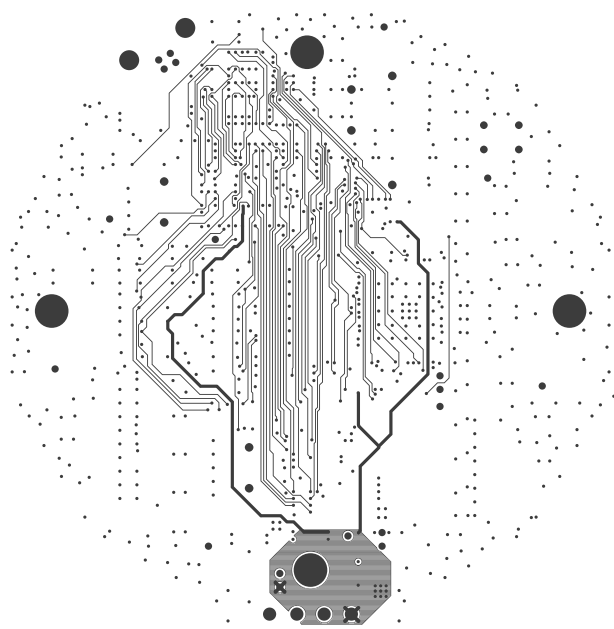


Figure 15. Layer 5

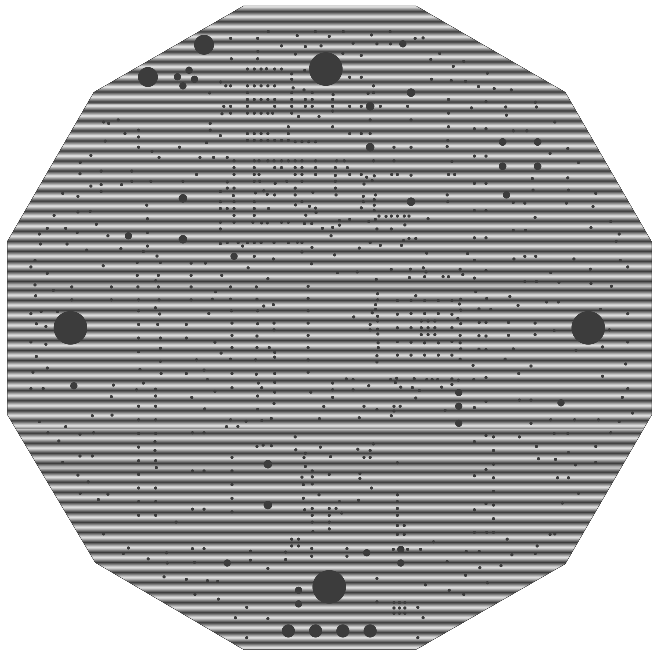


Figure 16. Layer 6, DUT Power

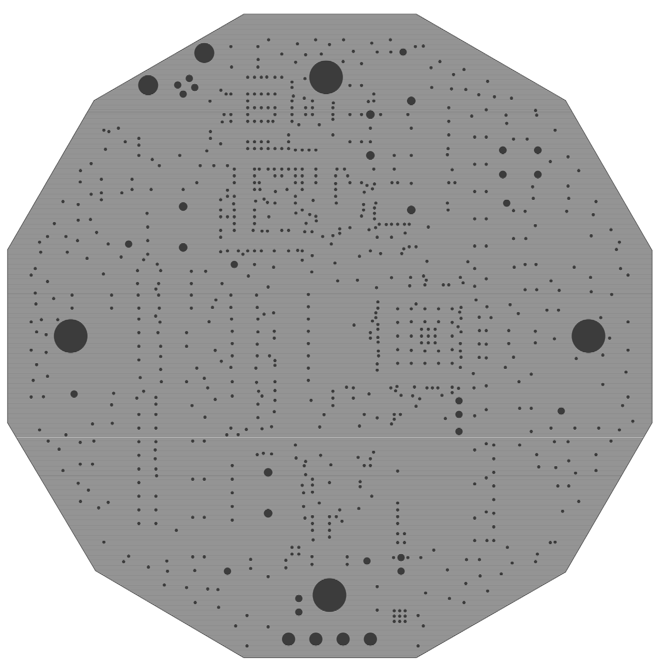


Figure 17. Layer 7, Ground Plane

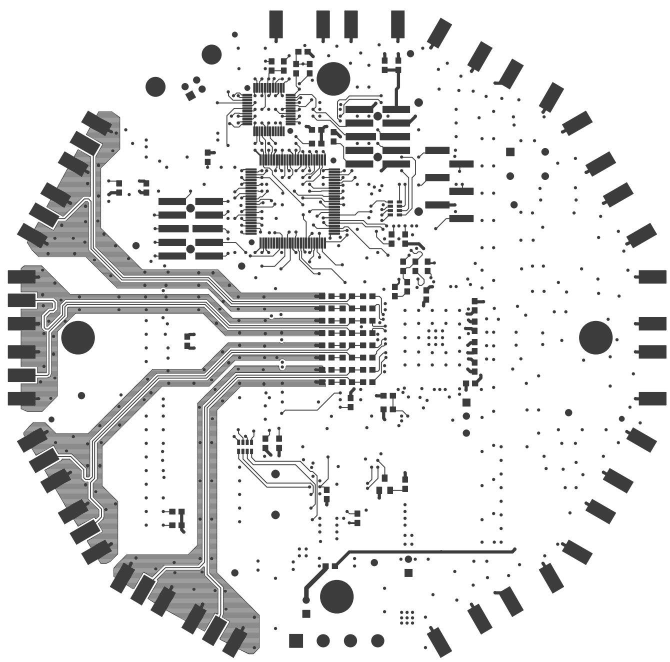


Figure 18. Layer 8

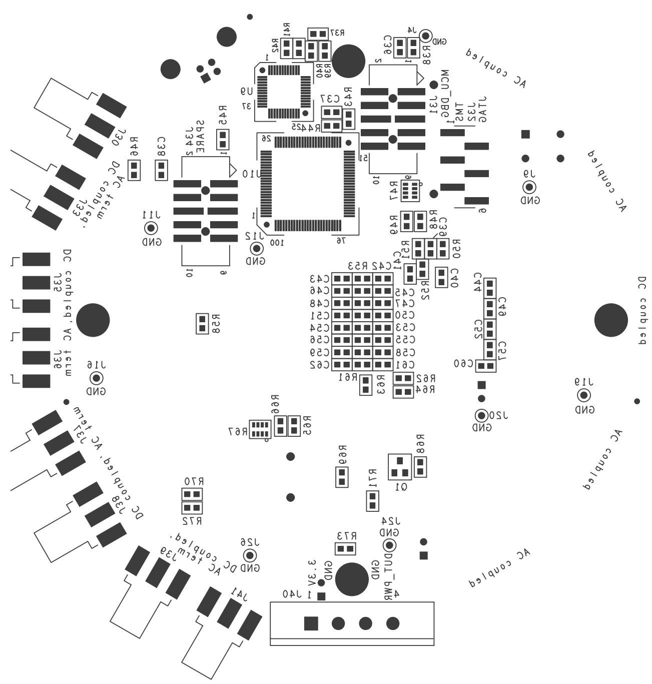


Figure 19. Silkscreen Bottom

Appendix—Powerup and Factory Default Settings

For the Si5367/68-EVB and the Si5369-EVB, the power up settings are as follows:

19.44 MHz input on either CKIN1, CKIN3 or CKIN4
CKIN2 is not used because of free run mode
155.52 MHz output on CKOUT1 and CKOUT2
622.08 MHz output on CKOUT3 and CKOUT4
311.04 MHz output on CKOUT5
Loop BW of 70 Hz for the Si5367/68-EVB; 4 Hz for the Si5369-EVB
LVEPCL outputs for CKIN1, CKIN2, CKIN3 and CKIN4

For the Si5365/66-EVB, the factory jumper settings are as follows:

For J17:

Silkscreen	Pin	Jumper	Comment
—	J17.1B	none	
AUTOSEL	J17.2B	none	Autosel, non-revert
FRQSEL0	J17.3B	none	
FRQSEL1	J17.4B	L	19.44 MHz in,
FRQSEL2	J17.5B	none	155.52 MHz out
FRQSEL3	J17.6B	L	
BWSEL0	J17.7B	L	lowest BW, 110 Hz
BWSEL1	J17.8B	H	
FRQTBL	J17.9B	L	SONET freq table
DBL2_BY	J17.10B	L	CK2OUT enabled
DBL_FS	J17.11B	L	FS_OUT normal
DIV34_0	J17.12B	none	CKOUT3, CKOUT4 = 77.76 MHz
DIV43_1	J17.13B	L	
SFOUT0	J17.14B	H	LVPECL out
SFOUT1	J17.15B	none	
RATE0	J17.16B	none	114.285 MHz xtal ref
RATE1	J17.17B	none	
FOS_CTL	J17.18B	L	FOS disabled
—	J17.19B	none	
—	J17.20B	none	

For J14:

Pin	Pin	Jumper	Comment
CS0_C3A	J14.1B	none	
CS1_C4A	J14.2B	none	
INC	J14.3B	none	
DEC	J14.4B	none	
—	J14.5B	none	
—	J14.6B	none	
DBL34	J14.7B	none	CKOUT3, CKOUT 4 enabled
FS_ALIGN	J14.8B	none	no FS alignment
FS_SW	J14.9B	none	CKIN3, CKIN 4 not LOS inputs
CK_CONF	J14.10B	none	no FS out alignment

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Updated "5.3.Si536x Input and Output Clocks" on page 5.
- Updated "5.5.MCU" on page 6.
- Added "Appendix—Powerup and Factory Default Settings" on page 26.

Revision 0.3 to Revision 0.4

- Updated for free run mode.

Revision 0.4 to Revision 0.5

- Added warning about low clock input frequencies to section "5.3.Si536x Input and Output Clocks" on page 5.
- Changed any-rate to any-frequency.
- Added the Si5369-EVB.

Revision 0.5 to Revision 0.6

- Removed software installation instructions and directed reader to refer to release CD or download from Silicon Labs web site.

NOTES:

CONTACT INFORMATION

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https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.